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Research Article

COMPARATIVE ANALYSIS OF DECIMAL ADDITION USING DIFFERENT TECHNIQUES

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ABSTRACT: Arithmetic operations of any of the digital devices like Calculator, computers, microcontrollers and other specialized digital systems are on Base 10 number system only. By Representing these kind of numbers in BCD the decimal precision applications has DSP, DIP are required in computer arithmetic. An adder for that kind of applications must have arithmetic modules that are worked based on coded decimal numbers and data as stored in the similar number format. In this paper, we proposed a decimal adder which is on FPGA based Mixed BCD/excess-6 technique that gives the better performance of decimal adders intended high-end FPGAs. We design adder with help of CLA(CLA), but in this paper we implement method decimal adder using carry increment adder (CIA) and to analyzing area and delay are compared with the existing decimal adder. The results of new decimal adder efficiently improved the features like area and delay. There are different types of possible decimal adder circuits, depending upon the code used to perform the decimal digits

Index Terms—Decimal addition, Carry increment adder (CIA),Carry look head adder(CLA),Field programmable gate array (FPGA), Exess-6, Binary coded decimal(BCD), Look up table(LUT).

I INTRODUCTION

Computer arithmetic is primarily depends on binary arithmetic since its numerical properties are easier to implement in hardware when it is represented in radix-2 than in base-10 [1][3]. However, the decimal arithmetic is a essential in the calculation of several applications, like commercial and financial, so that the results must be correspond to those which are done for human perceptions[13]. In several databases of these applications, the numbers are epitomized in form of decimal format only[5]. As we all know that the representation of many decimal numbers to exactly as binary numbers is not possible with a finite number of bits, in such cases arithmetic operations are to be performed directly on decimal numbers[2]. Decimal adder is used to add the decimal numbers. In general decimal numbers are added only when those decimal numbers are converting into binary coded decimal and then only we can add the numbers[7]. But it is easiest method used to add the decimal numbers directly which means there is no need of binary conversion[16]. It reduces the complexity and saves the time. In this way we indented a new decimal addition on mixed addition techniques with carry increment adder, to increase the delay and area of previous state of the art decimal adders.

Rest of the paper is systematized as follows, in section II we discussed about the earlier related works. In section III we discussed about the carry increment adder architecture, in section IV we portrayed the different designs of the Proposed Adder. The Results of the Proposed adder compared to the existing adder is accessible in section V and finally the paper concluded in section VI.

II LITERATURE SURVEY

Decimal arithmetic has built consideration in the field of computer arithmetic calculations due to the decimal particularly concern of application domains such as economic, marketable and internet[12]. In method Decimal Addition on FPGA, they propose a new technique that improves the orthodox decimal adders which aiming high-end FPGAs[2]. The method is based on a miscellaneous BCD / excess-6 illustration that allows adding two digits using only 4 LUT per digit plus two additional LUTs to convert the BCD / excess-6 digit to BCD, unlike previous solutions that require 5 LUT, by number, excluding conversion[6]. The method is based on a miscellaneous BCD / excess-6 representation that allows adding two digits using only 4 LUT per digit plus two additional LUTs to convert the BCD / excess-6 digit to BCD, unlike previous solutions that require 5 LUT, by number, excluding conversion. The consequences have been related with the best implementations of decimal adders. From the results, we conclude that the new adder has the best similarity of area and time. Compared to other multi-operator decimal adders, the proposed solution achieves roughly the similar time but with far fewer resources (about 25% reduces)[4]. The indented decimal adder also made it possible to design and implement a very efficient binary / decimal adder with the similar area and delay as a decimal adder.

III CARRY INCREMENT ADDER

The Carry Increment Adder involve of CLAs and incremental circuit[1]. The incremental circuit is composition by further half adders in Carry Look ahead chain with a successive request

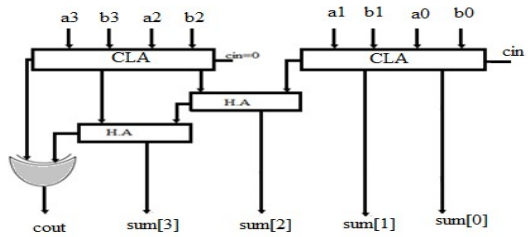

Fig.1. Block diagram of 4bit carry increment adder

The addition activity is finished by separating the maximum number binary of bits in to group of 2 bits and addition calculate is performed by a 2-bit CLA[14]. The particular, a 4-bit CIA includes two 2-bit CLA. The main block of CLA adds initial 2-bits to produce 2-bit sum and carry. Along with these, initial 2-bit addition of CIA was generated from 1st block of CLA[9]. Also, the carry output of 1st CLA block is given as input to the Cin of CIA circuit. Incremental circuit comprises of Half Adders. Thus, the partial sum generated from the 2nd CLA block is given to incremental circuit.

IV PROPOSED SINGLE DIGIT BCD ADDERS

To reduce the area and delay of the Conventional Adder we implement different types of techniques that is BCD adder, BCD & excess-6 adder and Excess-6 adder[15].

The design are name as 3 versions asdiscussed below

a.SINGLE DIGIT BCD ADDERS VERSION-1:

We designed BCD adder using Carry Increment Adder. Since BCD range is from 0 to 9.First we add unconditionally 6 to 'a' by doing this it will be in excess-6 representation. The output sum bits will be as follows

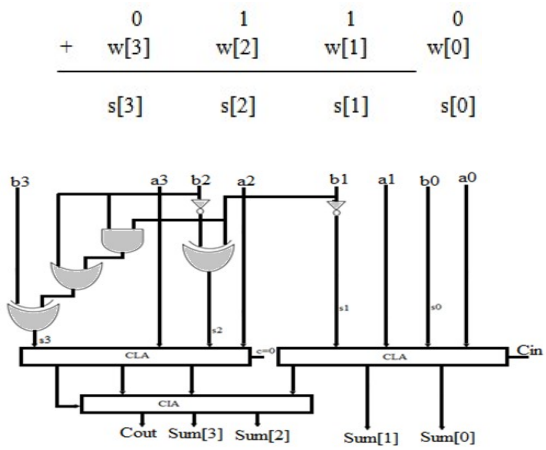

Fig. 2. Block diagram of single digit BCD adder version-1

From above equations to design single BCD adder with the help of CIA it depend upon 2-bit two RCAs and augmentation procedure is done by half adders[8]. The input of CIA 4-bit a & b limit is (a & b) є [0,9].One 4-bit binary data is added to 6 and this result is given to the RCA and another 4-bit binary data is given directly to Ripple Carry Adder. After performing Carry Increment Adder operation[11] we get 4-bit sum output. Based condition carryout the result is in excess-6 or BCD indicated as i.e. either Cout=0 result in excess-6 form or Cout=1 the results in BCD form. Similarly, we will perform the 2, 3, 4-digit BCD. Based on the design of 2, 3, 4 digit BCD we will check area and delay of the adders. In this identical method we can perform n-digit BCD.

b.SINGLE DIGIT BCD ADDER VERSION-2

In version-2, as a replacement for of adding 6 totally we will correct the result based on Cout is helping BCD converter[12]. To calculate Cout with the assistance of RCA, based on this carryout it will decide whether 6 has to be summed or not.

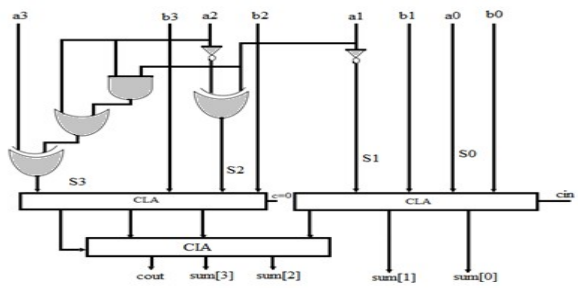

Fig.3 .Block diagram of single digit version-2

Suppose a pair of N-digit decimal number is represented in BCD

$$A = a_{N-1}, a_{N-2} \dots\dots\dots\dots\dots a1, a0$$

$$B = b_{N-1}, b_{N-2} \dots\dots\dots\dots\dots b1, b0$$

Here the addition operation $s = a + b + cin$ is employed with a fetter of 2xN digits to determine the BCD signal is followed by the summation of digits rendering to signal is BCD. Now the final result obtained is the decimal summation of N-BCD digits and carryout which is given by the last is BCD bit.

c.SINGLE DIGIT XS-6 ADDER VERSION-3

In version-3 we perform decimal addition with help of a single digit excess-6 representation, this excess-6 representation

is obtained by adding 6 to the BCD digits. For each 'a' and 'b' are in excess-6 representation[13]. To make the sum completely we are subtracting 6 from 'a' digit and that is as follows

	1	0	1	0
+	a[3]	a[2]	a[1]	a[0]
	s [3]	s[2]	s[1]	s[0]

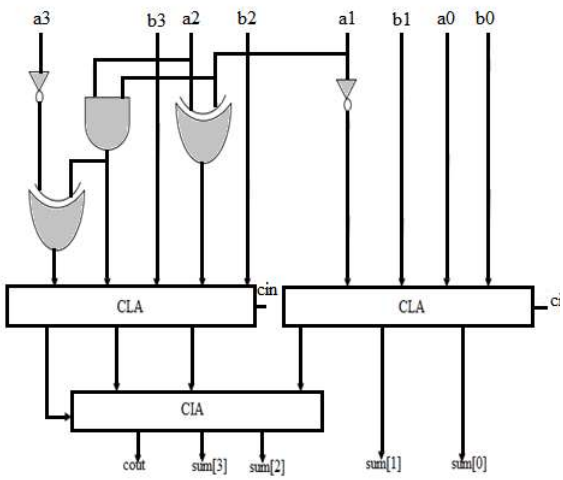

Fig. 4. Block diagram of single digit Excess-6 adder

From the above two excess-6 digits 'a' and 'b' are in the range of [6, 15].the result is obtained by subtracting 6 from 'a' then the output is represented as s=a-6 from the above equations. The final sum $s + b = a - 6 + b$ is obtained by performing the following equations.

V RESULTS AND DISCUSSION

We implemented proposed model of decimal adder using BCD/Excess-6 and performed 3 different versions with design 4-bit CIA. Intended for the design of carry increment adder 2 2-bit CLAs, 2 half adders and 2-bit x-or gate is used. The results are shown below

a. Version-1 Results:

In this version we implement the decimal addition by using the BCD adder, in this by adding the two BCD digits (0-9) Their sum is not in BCD. It can be overcomes this to add 6 to the one of the operand unconditionally if the results in the BCD for Example the representing the 10 in BCD is 0001 0000. The results is shown in the low figures. In these version we observed the delay and area of the single digit, two digits, third digits and four digits of decimal addition

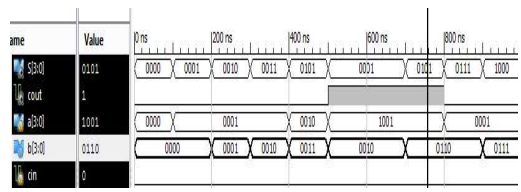

Fig. 5. Simulation Result of version-1

b. Version-2 Results

In this version we implement the decimal addition by using the BCD adder. It is similar to version-1 but small changes are done. In these version first we check the carry out, based on the carry out we can add the six with one of the operand added base on Cout. In the form of the BCD. In these version compare with the version-1 it can be some more better, the results are shown in the below figures, observe the delay and area of the single digit, two digits, third digits and four digits of decimal addition.

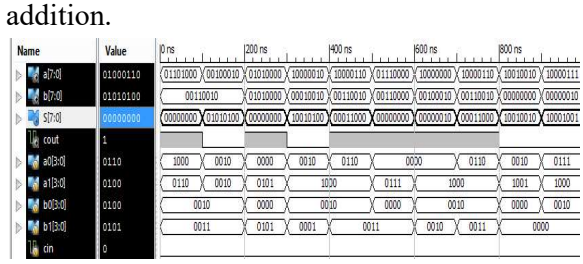

Fig. 6. Simulation Result of version-2

c. ***Version-3 Results***

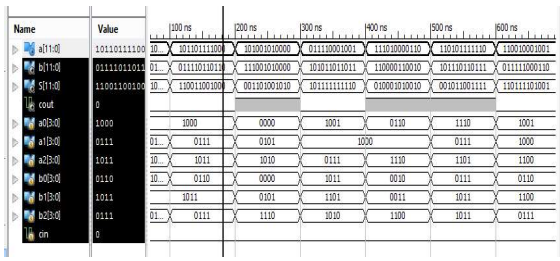

Fig 7: Simulation of version-3

Comparison of Results between Existing and proposed model:

The comparative analysis of decimal adder with help of BCD adder of version-1 is shown in below table 1.

Table-1 Comparison of version-1 Results

Type/parameters		Slices	LUT	IOB	Delay(ns)
CLA	1 digit	8	14	14	9.875
	2 digit	16	27	42	13.82
	3 digit	23	40	62	16.219
	4 digit	30	53	82	19.355
Carry Increment adder	1 digit	7	13	14	8.91
	2 digit	15	26	42	13.224
	3 digit	22	39	62	15.282
	4 digit	29	52	82	18.466

For the design of 1-digit BCD adder of version-1, CLA utilized 8 slices,14 LUTs and delay is 9.875ns.While coming to carry increment adder it utilized 7 slices,13 LUTs and delay is 8.91ns.In the similar way we designed 2-digit,3-digit and 4-digit and compared them. The above Table 1 clears the CIA (Carry increment adder) gives better results compared to CLA.

The comparative analysis of decimal adder with help of BCD adder of version-2 is shown in below table 2.For the design of 2-digit BCD adder of version-2, CLA utilized 12 slices, 22 LUTs and delay is 14.033ns.While coming to carry increment adder it utilized 11 slices,20 LUTs and delay is 13.897ns.

Table -2 Comparison of version-2 Results

Type/parameters		Slices	LUT	IOB	Delay(ns)
Carry Look Ahead Adder	1 digit	6	11	14	9.990
	2 digit	12	22	42	14.033
	3 digit	19	33	62	18.205
	4 digit	25	44	82	22.377
Carry Increment adder	1 digit	6	11	14	9.834
	2 digit	11	20	42	13.897
	3 digit	18	33	62	18.679
	4 digit	24	44	82	23.00

In the similar way we designed 1-digit,3-digit and 4-digit and compared them. By the analysis of the above Table 2 carry increment adder is gives better results comparing CLA.

The comparative analysis of decimal adder with help of Excess-6 adder is version-3and it is shown in below table 3. For the design of 3-digit BCD adder of version-3, CLA utilized 19 slices,34 LUTs and delay is 16.982ns.While coming to carry increment adder it utilized 19 slices,33 LUTs and delay is 15.511ns.

Table - 3: Comparison of version-3 Results

Type/parameters		Slices	LUT	IOB	Delay(ns)
Carry Look Ahead Adder	1 digit	6	11	14	9.353
	2 digit	12	20	42	13.802
	3 digit	19	34	62	16.982
	4 digit	22	41	82	18.376
Carry Increment adder	1 digit	6	11	14	9.621
	2 digit	13	22	42	13.108
	3 digit	19	33	62	15.511
	4 digit	22	39	82	17.117

In the similar way we designed 1-digit,3-digit and 4-digit and compared them. By the

analysis of the above Table 3 carry increment adder is performing better than CLA

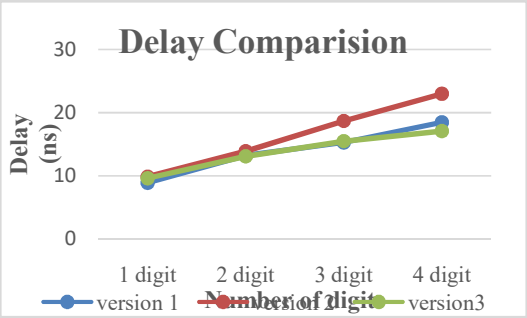

Fig-8 Comparison plot for proposed method

VI CONCLUSION

The implementation of decimal adder we fallowed the two types of techniques those are single digit BCD adder and single digit excess-6 adder by using these techniques we performed three versions. So with help of these versions we designed a decimal adder andthe technique uses the carry-chain significantly which is present in most FPGAs, as well as the supremecurrent devices. The carry-chain was familiarized in FPGAs for binary arithmetic design, The selected adder circuit with minimum area and delay is Carry Increment Adder for 4-bit in particular adders, and is now also used to get very efficient decimal adders. The results were compared with the existing and proposed model as of the results we conclude that the proposed adder had good performance in area and delay, when compared to other decimal adders, the proposed solution achieve the similar delay but with significantly less resources.

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