Research Article

QUALIFIED IMAGE WATERMARKING WITH APPROXIMATE ADDERS USING XILINX SYSTEM GENERATOR

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ABSTRACT:

Image security is playing a key role in present real world situations as the data transferring is mainly through digital images which may not secure. Hence, we present a novel algorithm for image watermarking using the error recovery adder and discrete wavelet transform. This process involves the hiding of one secret image into the host image qualitatively. For this process error recovery adder (ERA) is used to select the dynamic threshold value from the minimum values of the secret and host image. This error recovery adder reduces delay of the process. This work consists of both embedding and extraction process. The experimental consequences propose that the projected method provide results with high PSNR values.

Keywords: Image security, Error Recovery adder (ERA), discrete wavelet transform, Dynamic threshold.

I. INTRODUCTION:

At present days, communication via digital information become common due to its fast access. In modern communication, an extensive variety of technologies are needed for securing transmitting data from source to destination. Now a days, Digital media plays a vivacious role and also essential for hiding the content from the unofficial personals. For succeeding the important information must be embedded with some digital content for securing the information[1]. Hiding the data in some other data is known as watermarking [2-3]. Watermarking technique does not separate the watermark without changing the data even in the presence of different attacks.

Watermarking methods are classified based on different viewpoints. Depending on the viewpoint on how the original image is used throughout the procedure of watermark abstraction, it is classified in to blind and non-blind. Blind watermarking method is a method in which the host image is not used in the retrieving process, then it can be categorized as non- blind watermarking. Depending on the processing method used, watermarking methods are classified as spatial Domain and frequency domain.

Figure 1: Data hiding techniques

In the spatial method, directly pixel values of an image are modified. This method needs less computations, but less robust to attacks. In frequency domain techniques, frequency coefficients of an image are used for the embedding. These techniques are robust for

the attacks like rescaling, noise addition, lossy compression and Rotation.

In order to extract or embedded the image qualitatively the threshold has to be chosen to combine the low frequency bands of the watermark and host image [4]. The presence of static threshold leads to low quality of image. Hence, the threshold is selected dynamically based on the minimum intensity values of the host and watermark image using error recovery adders. The output of this adder s considered as the threshold.

The repose of this paper is ordered as follows. Section II presents the interrelated workings of proposed method. The proposed framework is depicted in Section III. Section IV provides the experimental results and Section V achieves the final process the paper.

II. RELATED WORK

A robust watermarking technique has detailed in [11] and is based on difference of corresponding coefficients between two successive DCT blocks. The host image is first split into 8x8 blocks tracked by use of DCT on each block. Based on the variance among dual corresponding coefficients of neighboring blocks watermark embedding is carried out. The technique shows ample amount of robustness against different attacks like cropping, rotation, JPEG Compression and some other singular attacks. But the drawback of the scheme is that it lacks the procedure tousle all the DCT blocks for embedding the watermark and hence embedding capacity is low. The technique has been improved and a better embedding capacity has been achieved in [12].

RAP-CLA, is an approximate adder based on the exact CLA, was proposed in [10]. This adder was able to modulate between the exact and approximate operating modes during the runtime. In RAP-CLA, fixed-size overlapped sub-blocks (windows) were used to compute the carry output and sum bits. Some multiplexers were used to provide accuracy re-configurability which resulted in higher delay, power, and area in the exact operating mode compared to those of a pure exact CLA. An approximate carry skip adder (ACSA), which divided an n-bit exact CSA adder into l-bit sub-adders, was suggested in [5]. The ACSA reduced the critical path length by using a carry prediction technique. In addition, ACSA proposed an error magnitude reduction unit to increase the output accuracy. Due to using the additional circuit, the power consumption became large. Also, ACSA had a long critical path and the error rate was high.

III. METHODOLOGY

The projected technique contains of the mainly two blocks. They are error recovery adder block and the DWT block. These blocks are explained below:

i. Error Recovery adder:

Approximate computation [5] the name itself refers to the approximation, it returns approximate results. Now a days, novel direction is approximate computing. In this method, errors are accepted because of its reducing the power. In many applications, such as audio, video, image processing, and machine learning, remarkable minor errors are certainly suitable. Those error tolerant applications are found in large quantity in initial applications and technologies.

Adders plays a dynamic role in arithmetic circuits. Adder performs addition of two binary numbers. RCA is the basic adder. The main demerit of this adder is each full adder has to wait until the carry of the previous adder generated. Through this process, delay

will occur. To overcome those problems, researches introduce several approximate adders [6], [7], [8], [9]. Through this adders, error rate will be high.

In our work, to minimize the error rate and delay by introducing a new adder which is ERA.

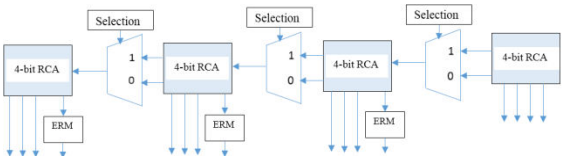

Figure 1: Architecture of ERA

The architecture of 16-bit ERA is illustrated in fig 4.In this adder, the four 4-bit RCA are considered. Here, the carry chain can be shortened for one block to another block by considering the input carry of present block through the inputs of the previous block. The carry can be selected based on the selection unit.

Thus the selection block output becomes K+G;

The mux inputs are

- Generation signal (G) (for 1) and the
- $P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$(For 0).

Where k is the kill bit, it can written as $\bar{A} + \bar{B}$ (next block first input position bits) and G is the generate signal as $A\&B$ (last bit position inputs of the previous block), P is the propagate signal as A xor B.

In this work, the error can be reduced by the proper selection of the carry. Therefore, reasons for the carry selection based on below four cases are explained in below.

Case 1 (when k=0, G=0): In this case the error can or can't be present. Therefore, the carry input of the present block may be propagated to its most significant bits. Hence, to reduce the probability of the error propagation in the proposed adder, in this case, the Select unit circuit, chooses the mux input (1) whose error probability is smaller than

Case 2 (when k=0, G=1):*G*is 1, the output of multiplexer is true. Then for this type of case carry is selected as G.

Case 3 (when k=1, G=0):when k=1, independent from the accuracy of next block carry input, the carry input is not propagated. Therefore, for shortening the critical path, we suggest to select input of 0 to mux as the carry output of the present block.

Case 4 (when k=1, G=1): It is similar to second case, G is 1, the mux output is correct. Hence for this purpose the carry is taken as G.

From the above cases, it is known that the carry is propagated only in case 1. Hence, the total length of the propagation of carry is restricted to only one block. In the third case, although the carry input of the block is killed and is not propagated, the carry input is employed to determine the first summation bit of the block. Therefore, if the carry input in this case is wrong, we suggest an error recovery unit which generates the first summation bit by

$$modified\ S_0 = (K.(P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0)) + (intial\ sum\ bit(S_0)) \quad --(1)$$

ii. Discrete wavelet transform:

The principal DWT was designed by Hungarian mathematician Alfred Haar. Inputs are symbolized as 2^nnumbers. This transform paired input vales and the sum values are passed after the difference was stored. This entire method is repeated upto the $2^n - 1$ alterations and an ending sum.

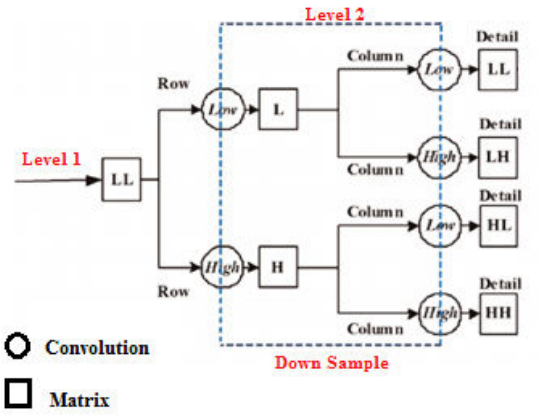

Figure 2: Block diagram of DWT

This work contains of doublestages image embedding and image extraction.

The flow for image embedding is given below:

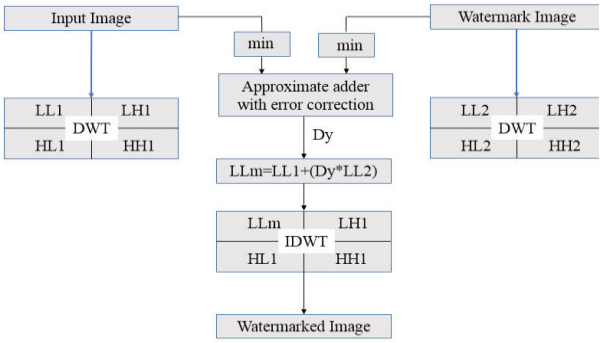

Figure 3: Flow of the image embedding process

Procedure:

- The input image and water mark image is selected.
- Then DWT is applied for both the input image and the secret image.
- The minimum values of the both images are taken and given as the input to the error recovery adder and the output obtained from this adder is selected as the dynamic threshold.

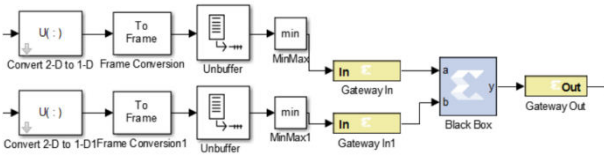

Figure 4: Error recovery block

- Then using this dynamic threshold and the LL bands of host and watermark images the new LL band is formed using the formula given:

$$LLm = LL1 + (Dy * LL2) --(2)$$

- Then apply IDW transform for the LLm, LH, HL, and HH from the host image.
- This block representation is given below:

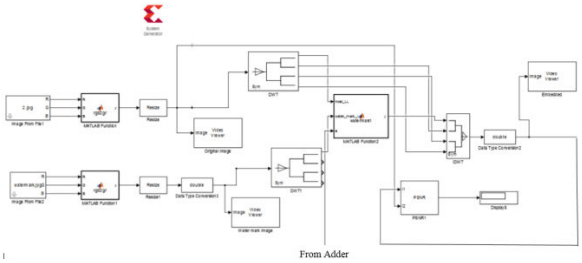

Figure 5: Block diagram of Embedding process

The extraction procedure of the projected work is given below:

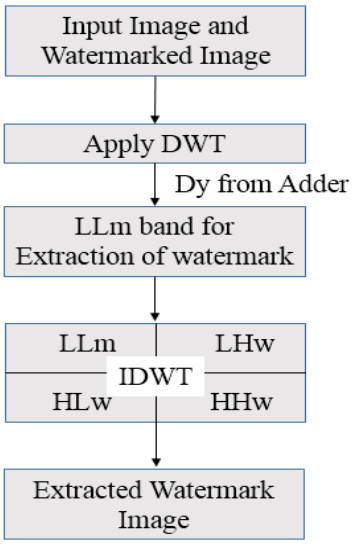

Figure 6: Flow of extraction process

Procedure:

- Similarly to embedding process, the threshold is selected dynamically using error recovery adder.
- Then the LL2 band is obtained from the equation as follows:

$$LL2 = \frac{LLm - LL2}{Dy} --(3)$$

- Then using tis LL2, LH, HL and HH of the watermark image the watermark is extracted using the idwt.
- The model for extraction is given below:

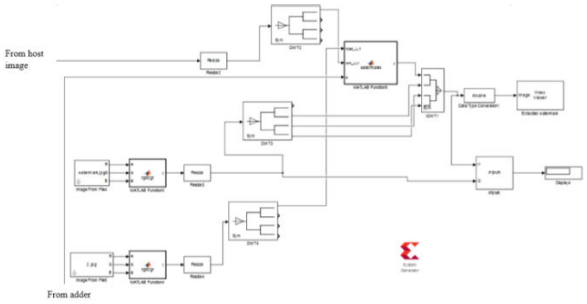

Figure 7: Block diagram of the Extraction process

IV. RESULTS

8(a) 8(b)

Figure: 8(a) implies the input image and 8(b) implies the Water mark image

9(a) 9(b)

Figure: 9(a) implies the embedded image and 9(b) implies the Extract Water mark image

PSNR values:

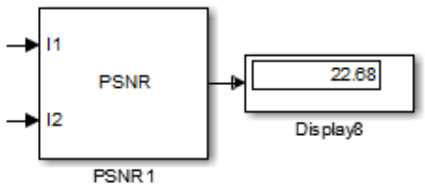

Figure 10: PSNR values of the Host and embedded image

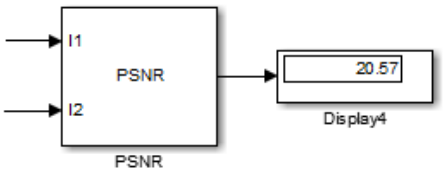

Figure 11: PSNR values of the secrete image and Extracted watermark image

V CONCLUSION:

In this paper, an efficient architectures for qualified image watermarking using error recovery adder was proposed. This worksuggests the adder based on approximation adder with recovery module which reduces worst case delay. The proposed technique are implemented using XSG. By using this adder the PSNR of the watermarking process will increase because of dynamic selection of threshold when compared to state of art methods.

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